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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,429	10/27/2000	Takenobu Tani	43889-992	4792

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	6

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,429	TANI, TAKENOBU	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Correspondence

1. This Office Action is taken in response to Applicant's filed application on December 10, 2003 in response to Official rejection dated September 10, 2003. Applicant's amendments and/or arguments have been considered with the results that follow.

Claims 1-9 are pending in the application under examination. No claims have been newly added or canceled.

Response to Arguments

2. Applicant's arguments filed December 10, 2003 have been fully considered but they are not persuasive for at least the following remarks.

Claims 1 and 8 require a read-only-memory (ROM) for storing instructions composing of a program and a modified instruction-storing unit for storing modified instructions for program modification. The Office Action provided reference (Jih (US 6,078,548)) featuring a read-only-memory (ROM) 10 for storing program codes and a random access memory (RAM) 20 for storing special instruction and modified program codes to addresses where the program codes are to be replaced. Applicant argues that the claims require '*an address translation unit outputting a substitutive address instead of an instruction address*' and contends that such requirement is missing from the applied reference. However, Jih pertinently teaches a special instruction-detecting unit detecting whether instruction is directed to a modified instruction or special instruction

such that a multiplexer is switched to the RAM. The RAM unit is provided for all modification to take place and from which the modified program codes stored are directly sent to be executed once the program counter directs to the memory address contain special instruction in the RAM. (See Col. 1, Line 62 to Col. 2, Line 12) It is simply common in computer architecture to redirect commands or instructions to updated instructions once the instructions have been updated.

Accordingly Jih does discloses, as required in the claims 1 and 8, a read-only-memory (ROM) for storing program codes and a random access memory (RAM) storing special instruction and modified program codes to addresses where the program codes are to be replaced, wherein the modified program codes stored are directly sent to be executed once the program counter directs to the memory address contain special instruction in the RAM. Therefore, it is again stated that the invention, as recited in claims 1-9 is anticipated over Jih (US 6,078,548) and the previous rejection is maintained and follows.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,078,548 (Jih).

With respect to claims 1 and 8, Jih teaches a microprocessor provided with a program modification function [(CPU capable of modifying built-in program codes thereof and method) title; abstract; Fig. 2], comprising: an instruction storage unit including a ROM for storing instructions composing a program to be processed (a read-only memory (ROM) 10 (FIG. 2) for storing program codes) and a modified instruction storage unit for storing a modified instruction for program modification (a random-access memory (RAM) 20 (FIG. 2) for storing a special instruction and modified program codes) [abstract; Fig. 2; Col. 1, Lines 56-61]; an address translation unit (special instruction detecting circuit) for receiving an instruction address of an instruction stored in said ROM and for translating the instruction address into a substitute address at which the modified instruction is stored in said modified instruction storage unit when the instruction address matches with a modified address which is an address of an instruction to be modified [30, FIG. 2; abstract; Col. 2, Lines 5-12], said address translation unit outputting the substitutive address to said instruction storage unit instead of the instruction address (special instruction detecting circuit connected to the ROM and the RAM to drive the CPU to transfer to read said modified program codes in the RAM when said special instruction is detected) [abstract; Col. 2, Lines 17-21; Col. 4, Lines 20-41].

With respect to claims 3 and 5, Jih teaches said address translation unit composed of a memory which outputs translated addresses in accordance with received instruction address [abstract; Col. 2, Lines 5-12] and address translation unit composed that a bit width to be a translation target is changeable when the instruction

address is translated into the substitutive address [abstract; Col. 2, Lines 22-29; Col. 4, Lines 21-47].

With respect to claims 2 and 4, said address translation unit comprising a modifying address storage unit for holding a value of a predetermined bit of the modifying address [Col. 3, Line 6-8, Lines 56-62]; an address comparator for comparing a value of said predetermined bit of the received instruction address with the value held in said modifying address storage unit to determine whether or not these values match (special instruction detecting circuit comprising comparators for comparing said selecting code and a higher bit of the address of the ROM to where the program counter directs) [Fig. 5; Col. Lines 19-34; Col. 4, Lines 20-27]; a substitutive address storage unit for holding a value of said predetermined bit of the substitutive address [Col. 3, Line 56 to Col. 4, Line 9]; and an address selector for receiving determination results of said address comparator, outputting as a value of said predetermined bit of a new instruction address, the value held in said substitutive address storage unit when the received results indicate a match, and otherwise the value of said predetermined bit of the instruction address (a multiplexer for passing the program codes in the ROM to execute in the normal operation, and to be switched to pass the modified program codes in the RAM to execute when the special instruction is detected) [Col. 4, Lines 1-19]; a translation range setting means capable of setting whether or not said predetermined bit is designated as a translation target bit, said address translation range setting means making said address selector output the value of said predetermined bit of the instruction address, regardless of the determination

results of said address comparator (determining number or regions and each region size) [Fig. 8; Col. 5, Lines 1-9].

With respect to claim 6, Jih teaches the address translation unit is composed of a field programmable logic which outputs translated address in accordance with received instruction address [Col 3, Line 62 to Col. 4, Line 9].

With respect to claims 7 and 9, Jih teaches said modified instruction storage unit stores an additional instruction for program modification and further stores a branch instruction having as a branch target an address of the additional instruction (special instruction is written in an address of the RAM corresponding to the memory address, where the program codes are to be replaced, of the ROM) [abstract; Col. 1, Line 59 to Col. 2, Line 12].

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,308.265 (Miller) teaching protection of boot code while allowing write accesses to the boot block.

US 6,253,281 (Hall) teaching method for updating firmware of a computer peripheral device.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

February 5, 2004